second via pattern and the third dielectric layer, and having a distance D between the first and second trench patterns wherein D exceeds WS;

C 6 cont.

h) anisotropically etching the first and second trench patterns through the third dielectric layer, thereby forming a first trench and a second trench, additionally forming a third and a fourth via pattern; and

i) anisotropically etching the third and fourth via patterns through the first dielectric layer, thereby forming a first via hole and a second via hole, wherein (1) the first trench and the first via hole are adapted for forming a first dual damascene structure and (2) the second trench and second via hole are adapted for forming a second dual damascene structure.

C7 24. (once amended) The method of claim 19 wherein D exceeds WS by at least 0.02μ.

Remarks

Claims 5, 11, 12, 13, 15, 19 and 24 have been amended.

✓ Claims 14, 21 and 31-42 have been cancelled.

Claims 1, 6-10, 16-18, 23 and 25-30 remain unchanged.

Applicant hereby requests further examination since applicant believes that the amendments to the claims and the claims remaining unchanged place the application in a condition for allowance.

I. Election/Restrictions

Applicant hereby cancels claims 33-42 since claims 33-42 are drawn to a nonelected invention.

II. Claim Rejections under 35 USC §112

The Examiner rejected claim 11 "under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention".[1]

Applicant has amended claim 11 by inserting the term "second" before the term "trench". Support for this amendment is found in clause j of claim 1. For the reason stated above, applicant believes that the 35 USC 112, second paragraph, rejection of claim 11 has been overcome. Applicant therefore believes that amended claim 11 is in a condition for allowance under 35 USC §112.

III. Claim Rejections under 35 USC §102(e)

A. The Examiner rejected claims 1, 5, 7-9 and 11-12 "under 35 USC 102(e) as being anticipated by Inohara et al [US 5,976,972]"[2]

Regarding to applicant's argument on pages 7-8 that "applicant sequentially forms first and second dielectric layer on a substrate without interposing a cap layer between the first dielectric and the substrate" and Inohara et al teaches "forms the via hole through the first dielectric layer and the cap layer" while "applicant's via hole that extends to the substrate is not formed through a cap layer"" the argument is not persuasive because the claim language does not excluding the step of forming a cap layer (claim 1 uses "the method comprising"). Rejection, therefore, is still proper.[3]

Applicant's claim 1 includes the following limitations

a) depositing a first dielectric layer on the substrate

i) anisotropically etching the second via pattern through the first dielectric layer, thereby forming a via hole extending to the substrate.

Applicant notes that the term "on" as recited in clause a) has a well defined meaning. See for example *Senmed Inc. v. Richard-Allen Medical Industries Inc.*, 12 USPQ2d 1508,

[1] Examiner's Detailed Action Memorandum, at item 2, p.2
[2] *Id., item 3, p.3*
[3] *Id., item 7, pp.11, 12*

1512, 1513 (Fed. Cir. 1989) holding that the claim language "on said anvil surface" means "in physical contact with" that surface. Additionally, it is well established that "'Words in a claim' will be given their ordinary and accustomed meaning unless it appears that the inventor used them differently.'" *See Envirotech Corp. v. Al George, Inc.*, 221 USPQ 473, 477 (Fed. Cir. 1984), citing with approval *Universal Oil Products Co. v. Globe Oil & Refining Co.*, 54 USPQ 504 (7th Cir. 1943), aff'd 61 USPQ 382 (1944). Regarding the ordinary and accustomed meaning of the term "on", applicant refers the Examiner to the dictionary meaning of this term, stating in part:

> **On** . . . ***prep.*** **1** in a position above, but in contact with and supported by; upon **2** in contact with (any surface); covering or attached to . . . (see Webster New World Dictionary, Third College Edition, Simon & Schuster, Inc. 1988, p.946).

Applicant notes that the courts have found that "texts such as dictionaries" may be required for claim construction " *C.E. Equipment Co. Inc. v. U.S.*, 13 USPQ2d 1363, 1367 (Cl. Ct. 1989).

In view of the above, applicant respectfully submits that claim construction of clause "a" of claim 1 means that the first dielectric layer is in contact with the substrate. If a cap layer is interposed between the first dielectric layer and the substrate, as suggested by the Examiner, the first dielectric layer cannot be in contact with the substrate. Additionally, if a cap layer were present between the substrate and the dielectric layer, the clause "j" limitation "etching the second via pattern through the first dielectric layer, *thereby* forming a via hole extending to the substrate" (emphasis added) would be inoperable. Regarding the examination of a patent application the court in *Ex parte Petersen*, 228 USPQ 216, 217 (BPAI 1985) stated "It is axiomatic that not only must claims be given their broadest reasonable interpretation consistent with the specification but also all limitations must be considered." More specifically regarding claim limitations in connection with the term comprising, the court in *Moleculon Research Corp. v. CBS, Inc.*, 229 USPQ 805, 812 (Fed. Cir. 1986) held "Whether structural recitation limits a claim depends on the language of the claim, the specification, prosecution history, and

other claims." Applicant notes that MPEP §2111.03 makes reference with approval to *Moleculon* regarding the meaning of the term comprising. In view of *Moleculon*, applicant respectfully submits that clause "a" provides a structural limitation to the term comprising, such that forming a cap layer is excluded from claim 1.

In view of the reasons provided above, applicant believes that it is inappropriate to construe claim 1 as additionally including the following steps: (1) depositing a cap layer on the substrate, (2) subsequently depositing a first dielectric layer on the cap layer and (3) anisotropically etching the second via pattern through the cap layer.

Anticipation under 35 USC §102 requires identity of invention in a single reference, see for example MPEP §2131, and it requires that "[A]n invention is anticipated if the same device, including all the claim limitations, is shown in a single prior art reference." *See Richardson v. Suzuki Motor Co. Ltd.,* 9 USPQ2d 1913, 1920 (Fed. Cir. 1980). It is well established that the courts apply a rigorous test for a finding of anticipation. "For a prior art reference to anticipate a claim, the reference must dislose each and every element of the claim *with sufficient clarity* to prove its existence in the prior art." *See Motorola Inc. v. Interdigital Corp.,* 43 USPQ2d 1481, 1490 (Fed. Cir. 1997) (emphasis added), making reference to *In re Spada*, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990). Furthermore, "[A]ny degree of physical difference, *however slight*, invalidates claims of anticipation. *See E.I. du Pont de Nemours & Co. v. Polaroid Graphics Imaging Inc.* 10 USPQ2d 1579, 1585 (D. Del 1989) (emphasis added), *aff'd* 13 USPQ 2d 1731 (Fed. Cir. 1989). Also, "[T]here is no anticipation 'unless all of the elements are found in exactly the same situation and united in the same way . . . in a single prior art reference.'" *See Perkin-Elmer Corp. v. Computervision Corp.*, 221 USPQ 669, 673 (Fed. Cir. 1984). Furthermore, the court in *Ex parte Lee* 31 USPQ2d 1105, 1110 (BPAI 1993), requires that an anticipatory reference under 35 USC §102 must be an identical disclosure "satisfying *each and every element* of the claimed invention" (emphasis in original).

Applicant is aware that anticipation need not necessarily be stated or provided expressly since the courts have found that "Anticipation can occur when a claimed limitation is

'inherent' or otherwise implicit in the relevant reference. *See Standard Havens Products, Inc. v. Gencor Industries Inc.,* 21 USPQ2d 1321, 1328 (Fed. Cir. 1991). The courts apply rigorous requirements to inherent anticipation, requiring that an element which is inherently asserted *must necessarily result* from the reference document. See for example *In re Oelrich and Divigard,* 212 USPQ 223, 326 (CCPA 1981) (emphasis in original):

> Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient. If, however, the disclosure is sufficient to show that the natural result flowing from the operation as taught would result in the performance of the questioned function, it seems to be well settled that the disclosure should be regarded as sufficient.

As reasoned above, applicant believes that it is inappropriate to include forming and etching a cap layer on the substrate in claim 1. Absent these cap layer related steps, Inohara et al. fails to meet the 35 USC §102 anticipation requirements such as those stated by the courts in *du Pont* "'A]ny degree of physical difference, however slight, invalidates claims of anticipation", *Perkin-Elmer* "[T]here is no anticipation 'unless all the elements are found in exactly the same situation and united in the same way . . . in a single prior art reference'.", and *Lee* requiring that the anticipatory reference must satisfy "each and every element of the claimed invention." Also, applicant respectfully submits that the claim 1 elements do not necessarily result from the Inohara et al. teachings. The Inohara et al. teachings thus fail to meet the *In re Oelrich* requirements for inherent anticipation.

For the reasons stated above, applicant believes that claim 1 is not anticipated by Inohara et al. Applicant therefore believes that claim 1 is in a condition for allowance under 35 USC §102(e).

Additionally regarding claim 1, the Examiner states "Moreover, the forming or not forming a cap layer depending on the design choice of a structure on a substrate is obvious for those skilled in the art."[4]

Applicant notes the Examiner's above quoted statement regarding obviousness fails to meet the requirements for anticipation under 35 USC §102(e) as enumerated above. However, in order to expedite prosecution, applicant is hereby responding to the Examiner's statement concerning obviousness of claim 1 wherein the Examiner deems claim 1 obvious as a "design choice".[5]

With regard to an obviousness rejection concerning a design choice, the court in *In re Chu*, 36 USPQ2d, 1089, 1094, 1095 (Fed. Cir. 1995), making reference to *In re Gal,* 25 USPQ2d 1076 (Fed. Cir. 1992), concluded a "finding of 'obvious design choice' precluded where the claimed structure and the function it performs are different from the prior art." The court in *In re Gal,* 25 USPQ2d 1076, 1077, 1078 (Fed. Cir. 1992) considered an obviousness rejection concerning an integrated circuit semiconductor chip, including patterned conductive and insulating layers (p. 1077) involving logic cells. The *Gal* court reversed the obviousness design choice rejection, finding the claim non-obvious due to the differences in functionality between the invention and the prior art concerning logic functionality and interconnectivity of integrated circuit transistors. Applicant's claim 1 includes forming patterned insulating layers and is adapted for fabricating a dual damascene structure. Dual damascene structures are widely utilized in integrated circuits, see for example applicant's application at page 1, lines 11 through 32. These dual damascene structures include conductive layers. Unlike the *Gal* invention, claim 1 does not include transistors or forming transistors. While the *Gal* invention concerns connectivity between interconnectivity between transistors, claim 1 concerns interconnectivity between layers, see for example clause "i" "etching the second via pattern through the first dielectric layer, thereby forming a via hole extending to the substrate." Also, there is a functionality difference between claim 1 and the "obvious

[4] *Id., at p.12*
[5] *Id.*

design choice" stated by the Examiner, since applicant's method is designed to etch through the first dielectric layer to the substrate, while applicant's method is not possible if a cap layer is interposed (as suggested by the Examiner) between the first dielectric layer and the substrate. By analogy with *In re Chu* and *In re Gal*, and for the reasons stated above, applicant respectfully submits that a design choice obviousness rejection of claim 1 would not be appropriate.

Regarding claim 5. Applicant has amended claim 5, making this an independent claim additionally including the limitations (1) recited in claim 1, (2) the substrate including at least one interconnect line, (3) depositing the first dielectric layer on the substrate and contacting the interconnect line, wherein the dielectric layer is deposited without any material layer interposed between the dielectric layer and the interconnect line. Support for this amendment is for example found in claim 1 and the specification at page 10, line 5 through page 12, line 9, and in FIGS. 5A – 5H.

Additionally regarding claim 5. Amended independent claim 5 includes each of the limitations recited in claim 1, Applicant believes that claim 1 is in a condition for allowance under USC §102(e), as reasoned above with respect to claim 1. Applicant therefore believes that amended independent claim 5 is in a condition for allowance under 35 USC §102(e).

Additionally, claim 5 includes the further limitations of having an interconnect line in the substrate, depositing the first layer on the interconnect line without interposing a material layer between the first dielectric layer and the substrate and etching a via hole through the first dielectric layer to the interconnect line.

Additionally, regarding the claim 5 limitation "wherein the first and third dielectric layers comprise material having similar etching characteristics." Inohara et al. teaches etching a wiring groove 46 and an opening region 51 in etch stop layer 44 and disclosing that "The etching progresses only through the opening region 41 overlapping the groove 46. Thus, a contact hole 48 reaching the stopper film 54 is formed along with the groove 46," see

Inohara et al. at column 13, lines 29-46 and Figs. 29 and 30. Inohara et al. discloses that the etching of the wiring groove 46 and the contact hole 48 is accomplished by RIE, but Inohara et al. does not teach or imply that the etching of wiring groove 46 and contact hole is accomplished in one continuous etching process or that Inohara et al. layers 44 and 45 employ materials having similar etching characteristics. Inohara et al. merely teaches forming the groove and the hole through RIE etching, thus lacking the recited limitation of claim 5. Applicant therefore believes that Inohara et al. does not meet the requirements for anticipation, either explicitly or inherently, under 35 USC §102(e). Applicant therefore believes that amended independent claim 5 is in a condition for allowance under 35 USC §102(e).

Regarding claims 7-9, and amended claims 11 and 12. Claims 7-9 and 11-12 depend from claim 1. Applicant believes that claim 1 is in a condition for allowance under 35 USC §102(e), as reasoned above. Applicant therefore believes that claims 7-9 and amended claims 11 and 12 are in a condition for allowance under 35 USC 102(e).

Additionally regarding amended claim 11. The Examiner states "filling the second trench and the via hole with a conductive material (49, Al-Cu, fig 32) (491-492, fig 32) whereby the dual damascene is formed." Applicant notes that applicant's via hole is etched through the first dielectric layer, thereby forming a via hole extending to the substrate (claim 1, clause i). In other words, the conductive material of claim 11 that is present in the via hole is deposited on the substrate without extending the via hole through a cap layer. Unlike claim 11, Inohara et al. extend the via hole through cap layer 54, thus failing to meet the requirements for anticipation under 35 USC §102(e) as enumerated in for example in *Motorola* and *du Pont*. Applicant therefore believes that amended claim 11 is in a condition for allowance under 35 USC §102(e).

Additionally regarding amended claim 12. Claim 12 has been amended to limit the conductive materials to metallic and non-metallic superconductors. Inohara et al. do not teach using metallic or non-metallic superconductors to form dual damascene structures. Applicant therefore believes that amended claim 12 is not anticipated by Inohara et al.

Applicant therefore believes that amended claim 12 is in a condition for allowance under 35 USC 102(e).

B. The Examiner rejected claims 13-14, 16-18 "under 35 USC 102(e) as being anticipated by Inohara et al [US 5,976,972]."[6]

Applicant has amended claim 13, adding the limitation that the distance between the first and second trenches exceeds the width of the sacrificial etch segment. Support for this amendment is found in the specification at page 16, lines 16-20. Applicant respectfully submits that Inohara et al. teaches forming a sacrificial etch segment that equals the distance between the first and second trenches, see for example Inohara et al. at Fig. 39 and Fig. 40. Applicant therefore believes that amended claim 13 is not anticipated by Inohara et al. Applicant therefore believes that, with respect to Inohara et al., amended claim 13 is allowable under 35 USC §102(e).

Regarding claims 16-18. Claims 16-18 depend from claim 13. As reasoned above, applicant believes that amended claim 13 is not anticipated by Inohara et al. Applicant therefore believes that, with respect to Inohara et al., claims 16-18 are allowable under 35 USC §102(e).

C. The Examiner rejected claims 13-14 and 16-18 "under 35 USC 102(e) as being anticipated by Lin [US 6,093,632]".[7]

Regarding claim 13. Applicant has additionally amended claim 13, adding the limitation that the widths of the first and second trench are narrower than the width of the first and second via etch patterns respectively. Support for this amendment is found in the specification at page 17, line 6 through page 18, line 16, Figs. 9A-9H and page 10, lines 10-32, Figs. 5B and 5C. Lin teaches forming via patterns (12a) and trenches (15b), wherein the via pattern width is narrower than the trench width, see for example column

[6] *Id., item 4, p. 4*
[7] *Id., item 5, p. 6*

5, lines 39-42 "Opening 12a, or the space between silicon nitride islands, which will subsequently translate to the diameter of the narrow diameter opening, of the dual damascene opening" and lines 56-61 "A selective, first RIE cycle, using CH_3 as an etchant, creates wide opening 15b, in silicon oxide layer 13, using opening 15a, in photoresist shape 14, as a mask, while creating narrow diameter opening 12b, in second silicon oxide layer 4, using opening 12a, located between small area silicon nitride islands 10b, as a mask", see Figs. 5-8. Applicant respectfully submits that the Lin via openings are narrower than the overlaying trench. Applicant therefore believes that amended claim 13 is not anticipated by Lin.

Additionally regarding claim 13, the Examiner has designated opening 12a as a sacrificial etch segment[8] and as a via opening[9]. Applicant is unable to discern this dual meaning in the teachings of Lin. The Examiner states that the Lin mask layer 11, Fig. 5, includes "a sacrificial etch pattern wherein the sacrificial etch pattern is positioned between the first and second via patterns."[10] However, Lin designates each 12a opening as a space between silicon nitride islands, which will subsequently translate to the diameter of the narrow diameter opening, of the dual damascene opening", see column 5, lines 39-42. Applicant respectfully submits that the Examiner's designation of opening 12a as a sacrificial etch segment and a via opening is inconsistent with the text of Lin. Also, the Examiner states with reference to Fig. 5, that "the sacrificial etch pattern is defined in the mask 11 for etching the etch stop layer at position not overlaying the interconnect structure 2 for reduced insulator capacitance by reducing areas of the etch stop layer 10a".[11] A review of Lin Fig. 6 shows that trench patterns 15 (layer 10a) are formed over the first and third openings 12b, but not over the center opening 12b. However, Figs. 7 and 8 show that center opening 12b has been widened to the same width as the adjacent trenches. Applicant respectfully submits that Fig. 6 is inconsistent with Figs. 7 and 8, with regard to the center opening, and is inconsistent with the text designating opening

[8] *Id.*
[9] *Id., item 7, p. 12*
[10] *Id., item 5, p. 6*
[11] *Id.*

12a as subsequently translating to the diameter of the narrow opening, of the dual damascene opening (column 5, lines 39-42). Due to inconsistencies between Fig. 6 and Figs. 7, 8 and the inconsistencies between Figs. 7, 8 and the text, applicant respectfully submits Figs. 6, 7 and 8 *mistakenly* show a center opening in layer 10a. Applicant thus believes that opening 12a does not designate a sacrificial etch opening and that Lin does not teach or disclose sacrificial etch openings. Applicant therefore believes that amended claim 13 is not anticipated by Lin and that amended claim 13 is thus, with respect to Lin, in a condition for allowance under 35 USC §102(e).

Additionally regarding issues concerning the center opening in layer 10a. Even if the center opening shown in Lin Figs. 7 and 8 were part of the Lin teachings, rather than a mistake in the drawings as applicant believes, applicant submits that these openings do not show a sacrificial etch segment since the Examiner has designated the (narrow) opening 12a (shown in Fig. 5) as the sacrificial etch segment. Also, there is no indication in the text or drawings how the center opening in layer 10a of Figs. 7 and 8 is formed, thus making the forming of this opening non-enabling. A prior art disclosure providing anticipation "must be such as will give possession of the invention to the person of ordinary skill". *See Paperless Accounting Inc. v. Bay Area Rapid Transit System,* 231 USPQ 649, 653 (Fed. Cir. 1986). The court in *Paperless* also stated "even if the claimed invention is disclosed in a printed publication, that disclosure will not suffice as prior art if it was not enabling". Also, concerning anticipation, see *Akzo N.V. v. U.S. International Trade Commission*, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986). "[T]he prior art reference must be enabling, thus placing the allegedly disclosed matter in the possession of the public". Applicant respectfully submits that Lin Figs. 7 and 8 are not anticipatory, because these figures are non-enabling with regard to the center opening in layer 10a. Applicant therefore believes that amended claim 13 is not anticipated by Lin.

As reasoned above, applicant believes that amended claim 13 is not anticipated by Inohara et al. and is not anticipated by Lin. Applicant therefore believes that amended claim 13 is in a condition for allowance under USC §102(e).

Regarding claims 16-18. Claims 16-18 depend form claim 13. As reasoned above, applicant believes that claim 13 is in a condition for allowance under 35 USC 102(e). Applicant therefore believes that claims 16-18 are in a condition for allowance under 35 USC §102(e).

D. The Examiner rejected claims 19, 21, 23 and 28-30 "under 35 USC. 102(e) as being anticipated by Lin [US 6,093,632]."[12]

Regarding claim 19. Applicant has amended claim 19, adding the limitation that (1) the widths of the first and second trenches is narrower than the width of the first and second via etch pattern respectively and (2) the distance between the first and second trenches exceeds the width of the sacrificial etch segment. Support for this amendment is found as described in applicant's Remarks Section III B and C above. Lin teaches forming via patterns (12a) and trenches (15b), wherein the via pattern width is narrower than the trench width, as reasoned above in applicant's Remarks Section III C. Additionally, applicant believes that Lin does not teach forming sacrificial etch segments as reasoned above in Remarks Section III C. For the reasons stated above, applicant believes that amended claim 19 is not anticipated by Lin. Applicant therefore believes that amended claim 19 is in a condition for allowance under 35 USC §102(e).

Regarding claims 23 and 28-30. Claims 23 and 28-30 depend from claim 19. Applicant believes that claim 19 is in a condition for allowance under 35 USC 102(e), as reasoned above. Applicant therefore believes that claims 23 and 28-30 are in a condition for allowance under 35 USC §102(e).

IV. Claim Rejections under 35 USC §103(a)

The Examiner rejected claims 6, 7-8, 10, 14-15, 24-27 and 31-32 "under 35 U.S.C. 103(a) as being unpatentable over Lin [6,093,632] in view of Inohara et al [US 5,976,972]".[13]

[12] *Id., item 4, p.7*
[13] *Id., item 6, p. 9*

Regarding claim 6, Applicant has amended claim 6, making claim 6 dependent from claim 1 and making the language of claim 6 consistent with the language recited in claim 1.

Regarding claims 6-8 and 10. Claims 6-8 and 10 depend from claim 1. Applicant believes that claim 1 is in a condition for allowance, see Remarks Section III A. Applicant therefore believes that claims 6-8 and 10 are in a condition for allowance.

Regarding claims 15 and 24-27. As reasoned in Remarks Section III C, applicant believes that Lin does not teach or disclose sacrificial etch openings. Applicant therefore believes that it is inappropriate to reject claims 15 and 24-27 over Lin in view of Inohara et al. Applicant therefore believes that claims 15 and 24-27 are in a condition for allowance under 35 USC §103(a)

Additionally regarding claim 15. Applicant has amended claim 15, making claim 15 dependent from claim 13 and making the language of claim 15 consistent with the language recited in claim 13. Applicant believes that claim 13 is in a condition for allowance, see Remarks Section III C. Applicant therefore believes that amended claim 15 is in a condition for allowance.

Additionally, regarding claim 24. Applicant has amended claim 24, making the language of claim 24 consistent with the language recited in claim 19. Claim 24 depends from claim 19. Applicant believes that claim 19 is in a condition for allowance, see Remarks Section III D. Applicant therefore believes that amended claim 24 is in a condition for allowance.

Additionally regarding claims 24-27. Claims 24-27 depend from claim 19. Applicant believes that claim 19 is in a condition for allowance, see Remarks Section III D. Applicant therefore believes that claims 24-27 are in a condition for allowance.

Version With Markings To Show Changes Made

IN THE CLAIMS

Please cancel claims 14, 21 and 31-42

Please amend the following claims as follows:

5. (once amended) A [The] method of [claim 1] forming a structure on a substrate including at least one interconnect line, the method comprising:

a) depositing a first dielectric layer on the substrate such that there is no material layer interposed between the interconnect line and the substrate;

b) depositing a second dielectric layer on the first dielectric layer, wherein the first and second dielectric layers comprise materials having dissimilar etching characteristics;

c) depositing a first mask layer on the second dielectric layer, wherein the first mask layer includes a first via pattern having a width T;

d) anisotropically etching the first via pattern through the second dielectric layer;

e) removing the first etch mask;

f) depositing a third dielectric layer on the second dielectric layer, wherein the second and third dielectric layers comprise materials having dissimilar etching characteristics and wherein the first and third dielectric layers comprise materials having similar etching characteristics;

g) depositing a second mask layer on the third dielectric layer, wherein the second mask layer includes a trench pattern overlaying the first via pattern and having a width P, such that T exceeds P;

h) anisotropically etching the trench pattern through the third dielectric layer, thereby forming (1) a first trench in the third dielectric layer and (2) a second via pattern;

i) anisotropically etching the second via pattern through the first dielectric layer, thereby forming a via hole extending to the interconnect line; and

j) anisotropically etching the first trench through the second dielectric layer, thereby forming a second trench extending through the second and third dielectric layers, wherein the via hole and second trench are adapted for fabricating a dual damascene structure.

11. (twice amended) The method of claim 1 additionally comprising simultaneously filling the second trench and the via hole with a conductive material, whereby a dual damascene structure is formed.

12. (once amended) The method of claim 11 wherein the conductive material comprises one or more materials selected from the group consisting of [metals, alloys,] metallic superconductors and nonmetallic superconductors having zero direct current resistance at or below their superconducting transition temperature.

13. (twice amended) A method of forming a structure on a substrate, the method comprising:

a) forming a dielectric stack including an etch stop layer;

b) depositing a first mask layer on the etch stop layer wherein the first mask includes: (1) a first via pattern having a width WV1, (2) a second via pattern having a width WV2 and (3) a sacrificial etch pattern positioned between the first and second via patterns such that the sacrificial etch pattern has a width WS [W];

c) anisotropically etching the first and second via patterns through the etch stop layer thereby extending the first and second via patterns through the etch stop layer and forming a sacrificial etch segment by

anisotropically etching the sacrificial etch pattern through the etch stop layer;

d) forming a first trench on the etch stop layer, such that the first trench does not overlay the sacrificial etch segment and wherein the first trench has a width WT1 that is narrower than WV1;

e) forming a second trench having a width WT2 on the etch stop layer, such that (1) the second trench does not overlay the sacrificial etch segment, [and] (2) the sacrificial etch segment is positioned between the first and second trenches, (3) the distance between the first and second trench exceeds WS and (4) WT2 is narrower than WV2;

f) forming a first via hole underlying the first trench, such that the first via hole communicates with the first trench and with the first via pattern extending through the etch stop layer; and

g) forming a second via hole underlying the second trench, such that the second via hole communicates with the second trench and with the second via pattern extending through the etch stop layer, wherein: (1) the first trench and the first via hole, and (2) the second trench and the second via hole area adapted for forming a first dual damascene structure and a second dual damascene structure respectively.

15. (once amended) The method of claim 13 [14] wherein the distance between the first and second trenches exceeds WS by [N is] at least 0.02μ.

19. (twice amended) A method of forming a structure on a substrate, the method comprising:

a) depositing a first dielectric layer on the substrate;

b) depositing a second dielectric layer on the first dielectric layer, wherein the first and second dielectric layers comprise materials having dissimilar etching characteristics;

c) depositing a first mask layer on the second dielectric layer wherein the first mask includes: (1) a first via pattern having a width WV1 [T], (2)

a second via pattern having a width WV2 and (3) a sacrificial etch pattern positioned between the first and second via patterns such that the sacrificial etch pattern has a width WS [W];

d) anisotropically etching the first and second via patterns through the second dielectric layer and forming a sacrificial etch segment by simultaneously anisotropically etching the sacrificial etch pattern through the second dielectric layer;

e) removing the first mask layer;

f) depositing a third dielectric layer on the second dielectric layer, wherein the second and third dielectric layers comprise materials having dissimilar etching characteristics;

g) depositing a second mask layer on the third dielectric layer, wherein the second mask layer includes: (1) a first trench pattern overlaying the first via pattern and the third dielectric layer, and having a width WT1 [P] and (2) a second trench pattern having a width WT2 overlaying the second via pattern and the third dielectric layer, and having a distance D between the first and second trench patterns wherein D exceeds WS [W by a measure N];

h) anisotropically etching the first and second trench patterns through the third dielectric layer, thereby forming a first trench and a second trench, additionally forming a third and a fourth via pattern; and

i) anisotropically etching the third and fourth via patterns through the first dielectric layer, thereby forming a first via hole and a second via hole, wherein (1) the first trench and the first via hole are adapted for forming a first dual damascene structure and (2) the second trench and second via hole are adapted for forming a second dual damascene structure.

24. (once amended) The method of claim 19 wherein D exceeds WS by [N is] at least 0.02μ.

In view of the above, applicant respectfully submits the claims remaining in the application are in a condition for allowance. The Examiner is invited to call the undersigned in the event the Examiner believes there are any outstanding issues remaining.

Respectfully submitted,

Dated: Dec. 18, 2001

By: Albert J. Dalhuisen

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